REMARKS

Claims 23-69 are pending in this case. Based upon the following remarks, it is respectfully submitted that these claims are allowable.

A. §103 Rejection

Claims 23-28, 30, 32-35, 38-44, 46, 48-51, 54-59, 61, 63-66 and 69 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jones et al., U.S. Patent No. 4,750,112 ("*Jones*"). This rejection is respectfully traversed and it is submitted that these claims recite subject matter which is patentable over *Jones*.

Regarding independent claims 23, 39 and 55, the Examiner contends, in part, that *Jones* teaches the following (with emphasis added):

> detecting an occurrence of a second combination of said respective states of said one or more clock control signals (signal from MicroCode Timing 12) [Fig. 3; col. 6, lines 41-45; Fig. 5; col. 8, lines 58-59] and in response thereto:
>
> interrupting said advancing of said sequence of instructions to said first pipeline subcircuit portion (the IP is idled or suspended) [col. 8, lines 59-61], followed by
>
> generating a plurality of address data [col. 2, lines 25-26];
>
> addressing said first pipeline subcircuit portion with said plurality of address data [col. 2, lines 33-41];
>
> executing with said second pipeline subcircuit portion a plurality of microcode (M1, M2, M3, etc.) substantially unrelated to said sequence of instructions in response to said enabled first clock signal [Fig. 5; col. 8, lines 58-59].

The Examiner contends further that although *Jones* does not explicitly teach that the first clock signal is disabled, one of ordinary skill in the art would have recognized that the clock signal is disabled during the idling, and that even if the clock signal is not disabled during the idling (emphasis added), it would have been obvious to one of ordinary skill in the art to disable the clock to conserve power.

According to the Examiner as quoted above, *Jones* teaches that the advancing of the sequence of instructions is interrupted by idling or suspending the "first pipeline subcircuit portion" (i.e., the IP, or "instruction pipeline", of *Jones*), following which that same "first pipeline subcircuit portion" is then addressed with the generated address data. However, that is not what *Jones* teaches. It is expressly taught at column 2, lines 33-41, of *Jones*, that it is the "execution pipeline", not the "instruction pipeline", that is addressed by the cited "address data". In any event, it is not understood how if the "first pipeline subcircuit portion" has been idled it can then be addressed anyway. Furthermore, *Jones* teaches at column 2, lines 22-26, that the "address data" is formed from instructions read from storage by the "instruction pipeline". However, if the advancing of the sequence of instructions is interrupted by idling or suspending the "instruction pipeline", as stated by the Examiner, then it is not understood how such instructions, now idled or suspended within the "instruction pipeline", can nonetheless be used to generate the "address data". The present claims expressly recite that the interrupting of the advancing of the sequence of instructions to the first pipeline subcircuit portion is followed by the generating of the plurality of address data.

Further according to the Examiner as quoted above, *Jones* teaches that the "second pipeline subcircuit portion" (i.e., the EP, or "execution pipeline", of *Jones*) executes a plurality of microcode in the form of M1, M2, M3, etc., which is substantially unrelated (emphasis added) to the sequence of instructions. However,

that is not what *Jones* teaches. At column 8, lines 47-50, *Jones* expressly states the following (with emphasis added): "I1-I25 represent machine instructions; M1-M6 represent additional microcode execution cycles required to complete the execution of a machine instruction". Hence, the cited microcode M1-M6 is not only not substantially unrelated, but is, to the contrary, substantially related since it is required to complete the execution of the machine instructions.

Regarding dependent claims 35, 51 and 66, which recite that the presently claimed method "further [comprises] asserting a status signal indicative of said disabling of said first clock signal", the Examiner has not identified and it is not understood where *Jones* teaches or suggests what may reasonably be considered an assertion of the presently recited "status signal".

Regarding dependent claims 30, 32, 46, 48, 61 and 63, the Examiner contends that *Jones* teaches that "prior to said executing of said plurality of microcode, completing executing of one or more of said advanced sequence of instructions which had been advanced to said first pipeline subcircuit portion prior to said detection of an occurrence of said second combination of said respective states of said one or more clock control signals". According to the Examiner, *Jones* teaches in Figure 5 that "instruction I5 is completely executed prior to the completion of microcode M2" (emphasis added). However, that is not what *Jones* teaches. At column 8, lines 58-64, *Jones* expressly teaches that instruction I5 requires an extra execution cycle (M2), and that microcode M2 is the second microcode step for instruction I5.

Regarding dependent claims 33, 34, 49, 50, 64 and 65, the Examiner contends that *Jones* teaches in Figure 5 that the first pipeline is re-enabled when the next instruction (I6) is detected. However, that is not what is presently claimed. These claims expressly recite "further comprising detecting another occurrence of said first combination of said respective states of said one or more clock control signals and in response thereto re-enabling said first clock signal"

(emphasis added). In other words, the re-enabling of the first clock signal is responsive to a detection of the first combination of the respective states of the one or more clock control signals, not to a detection of the next instruction.

B. Allowable Claims

Claims 29, 31, 36, 37, 45, 47, 52, 53, 60, 62, 67 and 68 were objected to as being dependent upon rejected base claims, but were identified as being allowable if rewritten in independent form to include all limitations of their respective base claims and any intervening claims. In view of the remarks in Part A hereinabove, it is respectfully submitted that these claims are not objectionable and are allowable.

C. Conclusion

Claims 23-69 remain pending in this case. Based upon the foregoing, it is respectfully submitted that these claims are allowable, and reconsideration and early allowance of these claims are requested.

Respectfully submitted,
VEDDER, PRICE, KAUFMAN & KAMMHOLZ, P.C.

Date: April 25, 2005 By: _____
Mark A. Dalla Valle
Reg. No. 34,147

Attorney for Assignee
222 N. LaSalle St., 24th Floor
Chicago, IL 60601
312-609-7500
Customer No.: 23,418